REMARKS

In the Office Action mailed June 4, 2003:

Claims 1, 6, 16 and 29-31 were rejected under 35 U.S.C. 102(b) as being anticipated by Nunomiya et al. (U.S. Patent No. 6,023,175).

Reconsideration of this rejection is respectfully requested.

Claims 2-5, 7-15, and 17-28 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35 U.S.C. 102(b) Rejection

Applicants' independent claim 1 claims an input buffer circuit comprising first and second differential input terminals, first and second differential amplifier circuits, and switches for selectively enabling the first differential amplifier circuit in a first input buffer mode and the second differential amplifier circuit in a second input buffer mode. First and second input signals are coupled, respectively, to the first differential input terminal and the second differential input terminal of the first and second differential amplifier circuits. As described below, the cited references do not anticipate these aspects of claim 1.

Nunomiya discloses a level interface circuit which receives "a first interface input signal having a level H and a level L, as fixed potentials, and a first reference level which is midway in between, or a second interface input having a level H and a level L and a second reference level". The level interface circuit "compares an input signal of one of said first and second interface input with one of said first and second reference level and generates an output signal". See Nunomiya Col. 2 lines 43-53 and Figure 1.

Nunomiya is distinguished from the disclosed input buffer circuit in that it does not process pairs of differential signals. As shown in Figure 1 of Nunomiya, the input signal received by the level interface circuit is a single-ended signal. The level interface circuit requires a reference voltage in order for it to operate. There is no common mode component between the input signal and the reference voltage. In contrast, the amplifier circuits of applicants' invention are designed to receive differential input signals in accordance with the

Low Voltage Differential Signaling (LVDS) standard (page 5, lines 23-24), which specifies a low noise, low power, and high-speed I/O interface that uses differential signals without a reference voltage. It requires two signal lines for each signal channel and the voltage difference between the two signal lines defines the logic stage of the LVDS signal (page 1, lines 15-18). Those skilled in the art would recognize that the input signals INA and INB of applicants' input buffer circuit are a pair of differential input signals, with common mode relationships between the two differential input signals. Having a differential pair of input signals enables the disclosed input buffer circuit not only to measure the amplitude difference, but also to measure the common mode difference between the two differential input signals (page 9 at line 7 and line 21), which is a capability the level interface circuit of Nunomiya does not have.

In addition, the reference voltage in Nunomiya is required to be set midway between two fixed potentials of the input signal, namely a H level and a L level. This limitation not only requires the input signal level to be within the H level and the L level, it also requires the reference voltage to be set precisely at the midpoint between the H level and the L level (see Nunomiya Col.2 lines 45-47 and claim 1). According to Nunomiya, the output signal would be asserted (digital signal level "1") if the voltage level of the input signal is higher than the voltage level of the reference voltage. The output signal would be de-asserted (digital signal level "0") if the voltage level of the input signal is lower than the voltage signal of the reference voltage. Unlike Nunomiya, applicants' input buffer circuit does not require the setting of a reference signal, and therefore does not limit the differential input signals to a fixed voltage range (between a H level and a L level). According to one embodiment of the disclosed input buffer circuit, the output signal would be asserted if the signal level of INB is larger than the signal level of INA, and the output signal would be de-asserted if the signal level of INB is smaller than the signal level of INA.

Referring to applicants' independent claim 29, this claim describes a method of receiving a signal transmitted according to one of a plurality of differential I/O standards. As discussed above, Nunomiya only describes a level interface circuit for converting a single-ended input signal to generate a level output signal. There is no discussion of any differential I/O standard by Nunomiya.

For the reasons presented above, Nunomiya does not anticipate the claimed limitations of the independent claims 1, 16 and 29 of the disclosed input buffer circuit. Therefore, Nunomiya does not anticipate the corresponding dependent claims 6, and 30-31 of the disclosed input buffer circuit.

Claims 2-5, 7-15 and 17-28 Objection

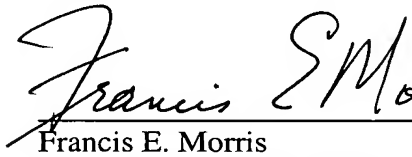
Claims 2, 7, and 17 have been rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claims 3-5 are dependent from claim 2, claims 8-15 are dependent from claim 7, and claims 18-28 are dependent from claim 17. In view of the indication that claims 2, 7, and 17 would be allowable if rewritten in independent form, all these claims are believed to be patentable.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully request the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims is not in condition for allowance, he is encouraged to phone the undersigned at (650) 849-7777 so that any remaining issues may be resolved.

No additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date: September 4, 2003



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